An 8.5kV Sacrificial Bypass Thyristor with Unprecedented Rupture Resilience

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***Abstract*—The paper details the development of a device intended for use as a sacrificial cell bypass switch in cascaded multi-level topologies with serial redundancy of cells of up to 4.6 kV (DC). The design is based on an 8.5 kV phase-control thyristor for industrial use. Maintaining rupture resilience constituted the main challenge. It ultimately triggered surges of more than 210 MA^{2}s without rupturing. Secondary challenges include a guaranteed surge *in*capability and ensuring a long-term stable short-circuit failure mode.**

I. Introduction

Modular Multi-level Converter topologies (MMC) can offer serial redundancy if a reliable means of discharging a faulty cell's energy storage and shorting its terminals is supplied. The stored energy in some high power applications is large enough to put the installation at risk when discharging due to the risk of semiconductor housing rupture, external arcing, capacitor explosion or electro-mechanical rupture of electrical connections. In many existing power systems, semiconductor explosions are accepted in fault cases because they cannot be avoided. Instead, explosions are contained and the cell terminals are shorted using a mechanical switch.

This work describes the development and application of a semiconductor-based bypass switch. This is not a new concept [1], [2], [3] but to the authors' knowledge, this publication marks the first time that all requirements for complete non-rupture conformance of the system have been addressed and fulfilled.

A. Intended application

In spite of having remarkable closing speed and non-rupture resilience, it is important to note that the device is *one* of the parts needed to achieve non-rupture conformance of the whole cell. The following is needed from the rest of the cell.

1) The active power semiconductor devices—switches and diodes—must retain non-rupture capability to some degree.
2) The control system must detect faults and trigger the bypass on a time-scale that doesn't allow other circuit elements to rupture.

Figure 1 illustrates a voltage-source MMC cell layout applicable for this device ("Bypass"). The choke ($\geq 3\mu$H) provides both surge-current moderation and slows the surge current transient. The cell controller (CC) detects faults by monitoring the choke voltage. The bypass control unit (not drawn) monitors the cell voltage and can trigger the bypass autonomously if the voltage exceeds safe limits; an ultimate safety measure in case of, for example, a defective cell controller. The inverting circuit (DC/AC conversion symbol) is typcally a half- or full-bridge, like in this work. More details on system ruggedness considerations can be found in [4].

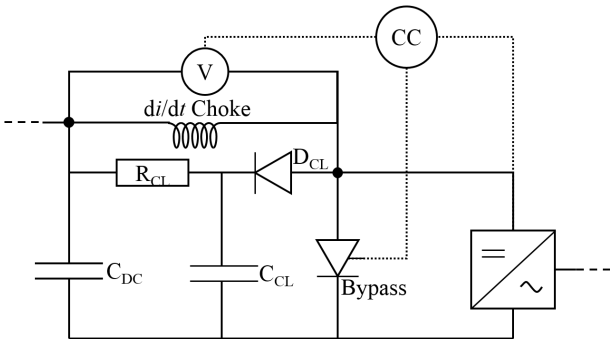

Fig. 1. The circuit diagram of a choked, voltage-source MMC cell of otherwise general architecture. The cell energy stored in C_{DC} can exceed 100 kJ. For a sense of the destructive potential, this energy is comparable to dropping the bypass thyristor from the top of Mount Everest.

B. Non-rupture criterion

Thyristor housing rupture is a concept standardised by IEC [5], and the ambition was to follow the standard as closely as possible. Most importantly, the housing technology for containing an unmitigated[1] edge arc at the targeted energy levels does not yet exist, assuming a reasonable device size. Spontaneous semiconductor failures *must* be mitigated, or explosions will inevitably occur. Two other aspects of the standard were disregarded. Firstly, IEC's test conditions were created with fused circuits in mind, which is why an application-specific fuse-free test circuit was developed. Secondly, the standard lists either loss of hermeticity after, or external detection of plasma during the surge as the rupture criterion, independent of the appearance of small cracks. As this work progressed, it became clear that it suffices to visually inspect the device after the surge, given that any optical

[1]The word "unmitigated" is used for arcs that are allowed burn in the device's internal air until the energy source is depleted without opening a parallel current path by triggering.

changes to the outside—e.g. ceramic hairline cracks or flange discoloration—are classified as ruptures.

II. Final design and performance

A. Wafer design

The wafer design is straightforward and based on an existing thyristor wafer type, exclusively for non-technical reasons. There are two challenges for the wafer: limiting the maximal surge-current capability to an acceptable level and steering spontaneous faults away from the wafer edge. The first challenge was met, while catastrophic edge faults could had to be mitigated by trigger assistance that guided the fault away from the edge.

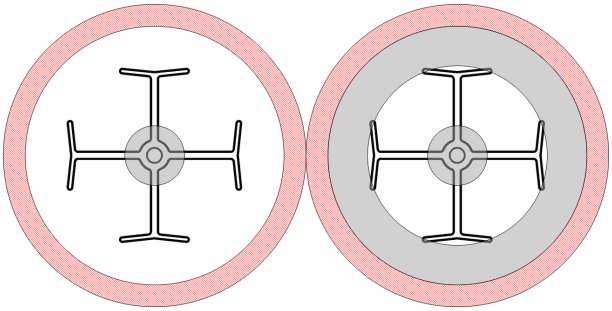

Fig. 2. Electron irradiation mask designs (light gray), overlaid with the wafer gate structure (black outline) and the silicone rubber (red striped fill). The left sketch shows the final design of the electron irradiation mask. To the right, the design of a two-part mask that was investigated but rejected, is shown.

The taken approach was to constrict the current to a small central portion of the wafer using a high-dose electron irradiation on the rest of the active area, shown in the left half of fig. 2. The on-state voltage increased to around 3 V at 100 A after irradiation. An unirradiated wafer would conduct thousands of Amperes at the same voltage. This irradiation led to a reasonably low maximal ITSM capability, needed for safe shorting of faulty cells without fully charged capacitors. It is an approximate 20 kA current pulse train shown in fig. 3. In the example, the device survives the first period (blocking the negative half-wave), but fails in the second positive half-wave at around 1.6 ms, seen as the sudden drop of the on-state voltage. The on-state voltage before triggering is incorrect (due to a measurement technicality) and should be disregarded. The test rig was set to pass three full periods through the DUT, which is why the oscillation ends at 3.3 ms.

The relatively rapid success of the approach led to limited investigation of other ideas and approaches. One approach that *was* investigated was to mask the electron irradiation also at the periphery of the active area, shown to the right of fig. 2. The motivating idea, loosely based on [6], was that the long lifetime region could self-trigger with help from the filament and move the arc into the active area. If this variant had any effect on the non-rupture capability of unmitigated edge-arcs, test resolution was too coarse to observe it, and it was abandoned because it increased the ITSM capability significantly.

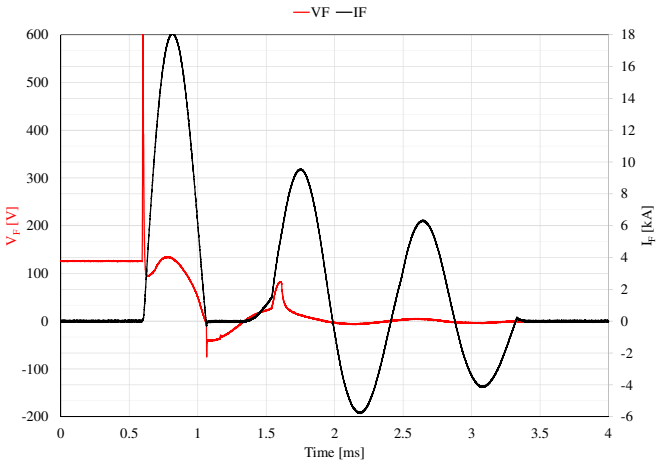

Fig. 3. Waveforms from a test of the minimal surge required to fail the bypass device.

The bypass device is operated at zero duty cycle under a DC-voltage that can reach 4.6kV. Avoiding numerous cosmic-ray failures forced the implementation of a wafer with 8.5kV blocking capability. Being a non-punch-through voltage design, such a wafer is quite thick—around 1.5 mm—and increases the on-state voltage of an electric arc, whose electrodes are separated by the wafer thickness. A designated bypass wafer design could be made using a punch-through inhibiting buffer thanks to the absence of reverse voltages in the intended application. This would allow for a thinner wafer to be used, maintaining cosmic-ray stability but with significantly lower energy absorption during a surge.

B. Housing design

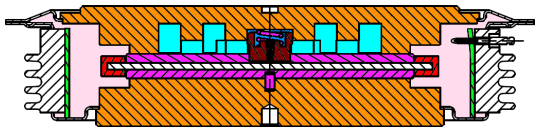

Fig. 4. Cross-sectional illustration of the assembled final housing.

Foregoing intermediate results, it was found that the most important aspect to achieve triggered non-rupture conformance at the highest energy levels was to make space inside the cathode pole-piece; an expansion volume that both decreases the gas pressure and improves heat transfer from the plasma to the cathode pole-piece. Figure 4 shows how the expansion volume (cyan) is included in the lid (upper orange region). The volume available for expansion in the original housing is indicated in dark blue colour—a minuscule region inside the gate contact—for visual comparison. Further improvements indicated in fig. 4 are: The ceramic walls are lined with a (green) silicone rubber strip, to protect the wall from cracking due plasma that may escape the pole-piece in spite of the expansion volume. The cathode sealing flange is somewhat protected by a labyrinth seal between the lid and the ceramic

wall. Finally, the external cathode centring bore was made shallower (the original bore is identical to that in the anode pole-piece), because a central arc could easily melt through the original weak-spot between the bore and gate contact seat. The design of fig. 4 passed all case non-rupture tests that the test rig could safely produce. The limitation corresponds to $i^2t \approx 215\mathrm{MA}^2\mathrm{s}$ and $\hat{\imath}_{\max} \approx 360$ kA, depending on the DUT impedance. The capability exceeds requirements, which is why it was not extended to provoke actual ruptures of the final design. The waveforms in fig. 5 is an example of a surge at the limit of the capability of the equipment.

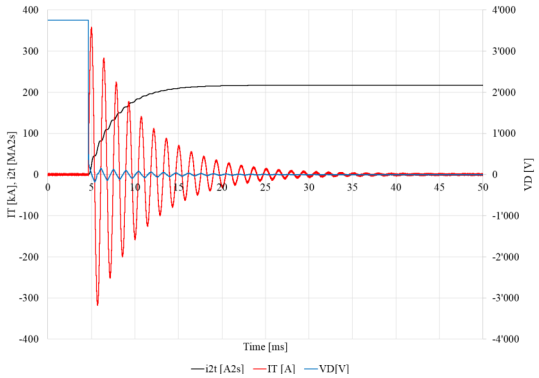

Fig. 5. Thyristor current and voltage wave-forms from the toughest surge the test rig could produce. $\hat{\imath}_{\max} = 363\mathrm{kA}$, $i^2t_{\max} = 217\mathrm{MA}^2\mathrm{s}$.

Figure 6 shows a 3D model of the developed lid to the left. In this illustration, the plasma expansion trenches are blue and connection trenches are green. The yellow area indicates the seal intended to keep the plasma in the expansion volume. The gate cable trench (red) breaches this seal, unfortunately, by necessity. A photography of the inside of a prototype lid after a maximally tough surge is shown to the right of fig. 6. Apart from noting that the hermetic seal was intact after the surge, there are a few observations to be made. First, the arc's pressure still sufficed to push the gate cable out of its trench. The amount of escaped plasma (and its temperature) did obviously not suffice to rupture the ceramic wall or the flanges, and is only visible as soot stains on the pole-piece at the mouth of the cable trench. It is also noteworthy that the labyrinth seal keeps the plasma from penetrating to the cathode flange where no soot stains are visible. However, since the anode flange is not protected by such a seal, the rupture capability (discoloration of the outside of the anode flange) could be quite close to the tested conditions. The insert in the lower right corner shows the inside of the anode flange, blackened by soot around the mouth of the gate trench.

III. Housing Design—Abandoned Concepts

The failed experiments are at least as interesting as the ultimate successful design. Figure 7 conveys an idea of how far from non-rupture conformance a device with damaged edge is, without any housing modifications or trigger-assist.

Attempts to reinforce the hermetic seal to allow unmitigated edge arcs all proved fruitless. The plasma is penetrant and

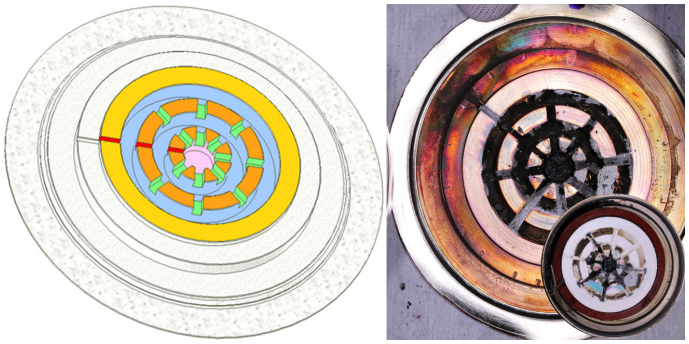

Fig. 6. A 3D illustration of the final lid (left). To the right, a photograph of the inside of a prototype lid after a maximally energetic surge. The insert shows cathode Moly-disc on top of the wafer and the rest of the anode-side assembly.

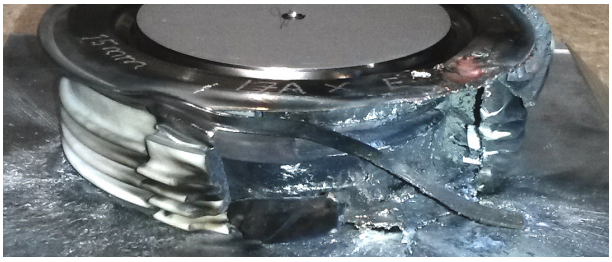

Fig. 7. One of the first non-rupture tests performed on a 102 mm housing with an unmitigated edge failure. $\hat{\imath}_{\max} = 199$ kA and $i^2t = 37\mathrm{MA}^2\mathrm{s}$.

aggressive, finding its way past obstacles to a point where the shielding effort becomes too expensive or difficult to manufacture. As a result, the unmitigated edge arc requirement was abandoned for the housing, and trigger assistance was designed into the control circuit. The arc is reliably moved from the periphery to the centre of the device if triggered quickly enough. However, even with a central arc, non-rupture conformance proved non-trivial or even difficult. The reason is that there is almost no volume available for plasma expansion in the original housing. The original available volume is a subset of the final housing cross-section, indicated in fig. 4 as blue areas around inside the gate contact. Lacking expansion volume, the plasma creates the following paths to either the internal or external atmosphere:

- Primarily, it flows through the channel made for routing the gate lead through the pole-piece, erratically pushing the gate lead out of the channel, which widens the path. All attempts to close the channel, using resins and metals, failed.
- The original housing lid had a deep external centring bore in the cathode pole-piece. The arc easily melted the weak spot between the bore and the gate contact seat, creating a path to the outside. By decreasing the depth of the centring bore, the path was closed.
- A few observations suggest that the plasma pressure trumped the contact force (40kN), resulting in a temporary separation of the pole-pieces that would increase contact resistance and the thyristor's absorbed share of

the stored energy.

Three housing sizes (102, 120 and 150 mm flange outer diameters) were fitted for the selected wafer size ($\oslash \approx 75$ mm). The expansion trenches were only tested with the 120 mm housing. There is tendency towards better performance with increasing housing size which suggests that an arbitrarily large housing would meet expectations at some point. This tendency is illustrated in fig. 8, showing how a triggered surge causes an explosion in the 102 mm housing in the upper half, compared to the slight cracking of the ceramic wall of a 150 mm housing, barely visible on the outside ceramic wall. While both surge events lead to ejection of the gate cable and were classified as ruptures, the plasma obviously loses some of its destructive potential on its way to the wall of the larger housing. The bottom picture shows the coiled-up gate cable resulting from being pushed out of the trench by the explosion.

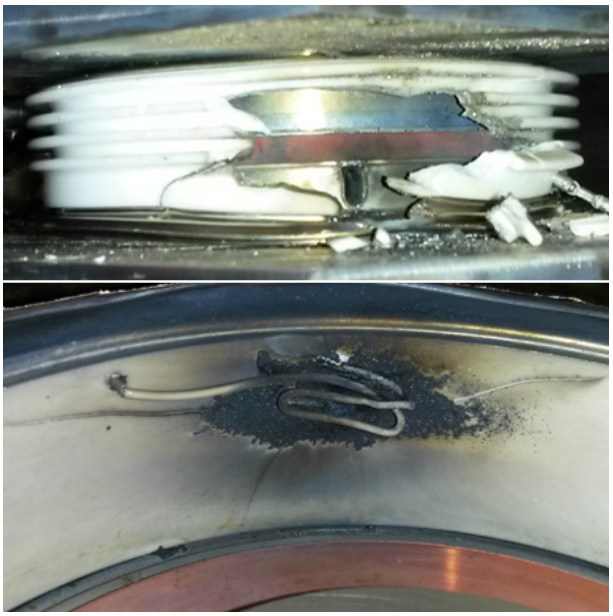

Fig. 8. Post-surge photographs of a 102 mm housing (top), compared to a 150 mm housing (bottom). The bottom picture is taken after the housing was opened, at the inner ceramic wall in the direction of the gate cable trench.

Early housing rupture testing often yielded erratic results, changing dramatically with the incorporation of plasma expansion trenches for which no single rupture was observed. Part of the explanation is surely that testing with high resolution is laborious and expensive. A device can only be tested once, regardless of whether it passes or fails. If conditions are far away from the capability in any direction, much detail is lost. But it must also be admitted that plasma behaviour is complex and that there probably were influential parameters that were not controlled in the experiments.

IV. Reliability

Device requirements in operation are trivial in comparison to other devices. Thanks to the low active losses, the device assumes approximately the ambient temperature in operation, leading to trivial load- and temperature cycling requirements.

After triggering, its short-circuit failure mode (SCFM) remain low-ohmic until the next planned maintenance. To verify the stability, SCFM testing was performed at maximal foreseen phase current, 1300 A_{RMS}, for over a year. A range of different variants were tested, both hermetic and punctured, with and without the wafer sandwiched between 0.5 mm thick Aluminium foils. While all tests passed the test electrically with monotonous on-state voltages varying between 0.1 and 1.75 V, the appearance after the test varied substantially. The use of Aluminium foils had a tremendous impact on the post-SCFM appearance. Two extremes are shown in fig. 9. Interestingly, these devices display similar electrical behaviour in spite of the standard-assembly wafer melting completely. However, the use of foils could not be motivated in the final design, since it did not improve electrical SCFM performance measurably.

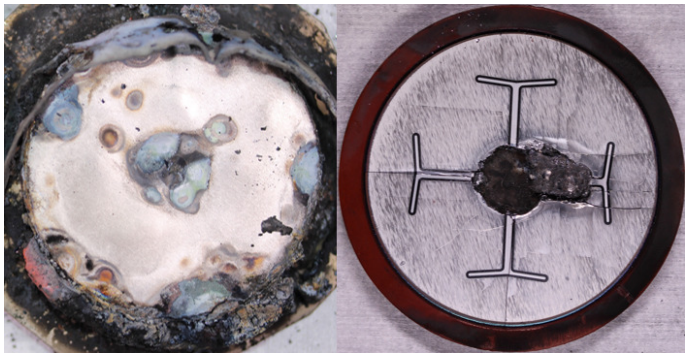

Fig. 9. Two wafers after one year in SCFM at 1300 A_{RMS}, both wtih punctured, non-hermetic, housings. The wafer to the right was sandwiched between two 0.5 mm thick Aluminum sheets. The wafer to the left had a standard assembly, the only identifiable remains being a bit of red rubber in the lower left corner.

V. Conclusion

A semiconductor-based bypass device for use in Modular Multilevel Converter topologies with a cell voltage of up to 4.6kV DC is proposed. The device will not rupture up to or exceeding 363 kA or 217 MA^2s, as long as it is triggered during the fault. The key to achieving such high non-rupture ratings is to provide volume inside the pole-piece for the byproducts of the electric arc to expand and cool. After a fault, the device displays a stable short circuit for more than a year under 1300 A_{RMS} at a voltage drop below 1.75 V_{RMS}.

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CITATION
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